CLAIMS

What is claimed is:

1. A method for fabricating a semiconductor product comprising:

providing an embedded semiconductor product comprising:

an embedded logic region having formed therein a logic field effect transistor device;

an embedded memory region having formed therein a memory field effect transistor device; and

a kerf region having formed therein a kerf field effect transistor device; and

measuring for the embedded semiconductor product a gate electrode linewidth for each of the logic field effect transistor device, the memory field effect transistor device and the kerf field effect transistor device.

2. The method of claim 1 wherein each of the logic field effect transistor device, the memory field effect transistor device and the kerf field effect transistor device has a linewidth of from about 0.05 to about 0.15 microns.

3. The method of claim 1 wherein each of the logic field effect transistor device and the memory field effect transistor device has a gate electrode linewidth:separation distance ratio of from about 1:1 to about 1:1000.

4. The method of claim 1 wherein the embedded semiconductor product further comprises a non-kerf and non-embedded region having formed therein a non-kerf and non-embedded field effect transistor device.

5. The method of claim 4 further comprising measuring a gate electrode linewidth of the non-kerf and non-embedded field effect transistor device.

6. A method for fabricating a semiconductor product comprising:

providing an embedded semiconductor product comprising:

an embedded logic region having formed therein a logic field effect transistor device;

an embedded memory region having formed therein a memory field effect transistor device; and

a kerf region having formed therein a kerf field effect transistor device;

measuring for the embedded semiconductor product a gate electrode linewidth for each of the logic field effect transistor device, the memory field effect transistor device and the kerf field effect transistor device; and

comparing the gate electrode linewidths for each of the logic field effect transistor device, the memory field effect transistor device and the kerf field effect transistor device.

7. The method of claim 6 wherein each of the logic field effect transistor device, the memory field effect transistor device and the kerf field effect transistor device has a linewidth of from about 0.05 to about 0.15 microns.

8. The method of claim 6 wherein each of the logic field effect transistor device and the memory field effect transistor device has a gate electrode linewidth:separation distance ratio of from about 1:1 to about 1:1000.

9. The method of claim 6 wherein the measured gate electrode linewidths are compared among themselves.

10. The method of claim 6 wherein the measured gate electrode linewidths are compared to specified target values.

11. The method of claim 6 wherein the embedded semiconductor product further comprises a non-kerf and non-embedded region having formed therein a non-kerf and non-embedded field effect transistor device.

12. The method of claim 11 further comprising measuring a gate electrode linewidth of the non-kerf and non-embedded field effect transistor device.

13. A method for fabricating a semiconductor product comprising:

providing an embedded semiconductor product comprising:

an embedded logic region having formed therein a logic field effect transistor device;

an embedded memory region having formed therein a memory field effect transistor device; and

a kerf region having formed therein a kerf field effect transistor device;

measuring for the embedded semiconductor product a gate electrode linewidth for each of the logic field effect transistor device, the memory field effect transistor device and the kerf field effect transistor device;

comparing the gate electrode linewidths for each of the logic field effect transistor device, the memory field effect transistor device and the kerf field effect transistor device to specified target values to determine a set of deviations therefrom; and

fabricating a second embedded semiconductor product while adjusting at least one of a mask pattern dimension and an exposure condition such as to compensate for the set of deviations.

14. The method of claim 13 wherein each of the logic field effect transistor device, the memory field effect transistor device and the kerf field effect transistor device has a linewidth of from about 0.05 to about 0.15 microns.

15. The method of claim 13 wherein each of the logic field effect transistor device and the memory field effect transistor device has a gate electrode linewidth:separation distance ratio of from about 1:1 to about 1:1000.

16. The method of claim 13 wherein the embedded semiconductor product further comprises a non-kerf and non-embedded region having formed therein a non-kerf and non-embedded field effect transistor device.

17. The method of claim 16 further comprising measuring a gate electrode linewidth of the non-kerf and non-embedded field effect transistor device.

18. The method of claim 13 wherein only the mask pattern dimension is adjusted.

19. The method of claim 13 wherein only the photoexposure condition is adjusted.

20. The method of claim 13 wherein both of the mask pattern dimension and the photoexposure condition are adjusted.